

VIDEO PERCEPTION INCORPORATED

IPP4200R

CMOS REAL TIME BOUNDARY LOCATOR

The IPP4200R provides boundary locations of all objects in a video scene. It communicates these relatively low volume data to the external memory storage of a controlling processor. This enables the controlling processor to quickly locate an object. The data content permits location of scene position and orientation. The IPP4200R is a uniquely programmed device that loads an Altera 10K10 Programmable Logic Device (PLD); the PLD is user supplied. The PLD functions as an IPP4200 when powered-up (loaded with the IPP4200R program). A small external RAM is required for support to permit this 3-component set to function with minimal interface to the user system.

The video scene is divided into 4 x 4 pixels areas called cells. The IPP4200 evaluates each cell to determine if it has a boundary (edge) of an object within the cell. The true/false (boolean) status is registered for each cell; 16 pixels are represented by a single bit. The IPP4200 accepts digitized video data and translates these to cell status with inherent image noise filtering and image enhancement. A 16-bit word representing the status of 16 cells is output to the controlling processor system memory. This process is continuously repeated as the field of video data is scanned.

The transfer time (of the 16-bit output) is only a very small percentage of the scan time of the field. The delay time (from the scanning of a pixel to the output of status data) is less than the time for eight horizontal line scans. This permits the use of this device in a pipeline processing system. The IPP4200 can be externally controlled to change a differential threshold level controlling sensitivity. It processes digitized video camera data in real time with minimal data storage to RAM. It supports a maximum image horizontal line size of 1024 pixels while self-adjusting to any shorter line. There are no size limitations in the vertical direction permitting it to be used for both linear array and two dimension video cameras. The device operates up to 25MHz (preliminary) pixel clock rate.

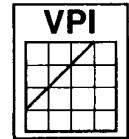
The IPP4200 detects objects of a minimum size of 4-pixels in either the horizontal or vertical direction. **The IPP4200 provides a coordinate-structured (x, y) output format; it can identify the location of objects in a real time system. It translates these data in a condensed, quickly interpreted format to a controlling system computer.**

FEATURES

- Locates Boundaries (Edges)
- Performs Both Horizontal and Vertical Scanned Edge Detection
- Translates Image to Condensed Form Compatible with Computer
- Condenses Image to 1 Bit Per 16 Pixels
- Performs Serial-to-Parallel Conversion for 16 Bit Output
- Operates at 25 MHz Pixel Clock Rate
- Provides Real Time Image Processing
- Filters Image Noise
- Enhances Image Boundary
- Provides up to 1024 x 1024 Processing Resolution
- Supports Both Linear Array and Two Dimension Video Cameras
- Supports Camera-Based or External-to-Computer Usage
- Supports Dynamic Differential Threshold Adjustment

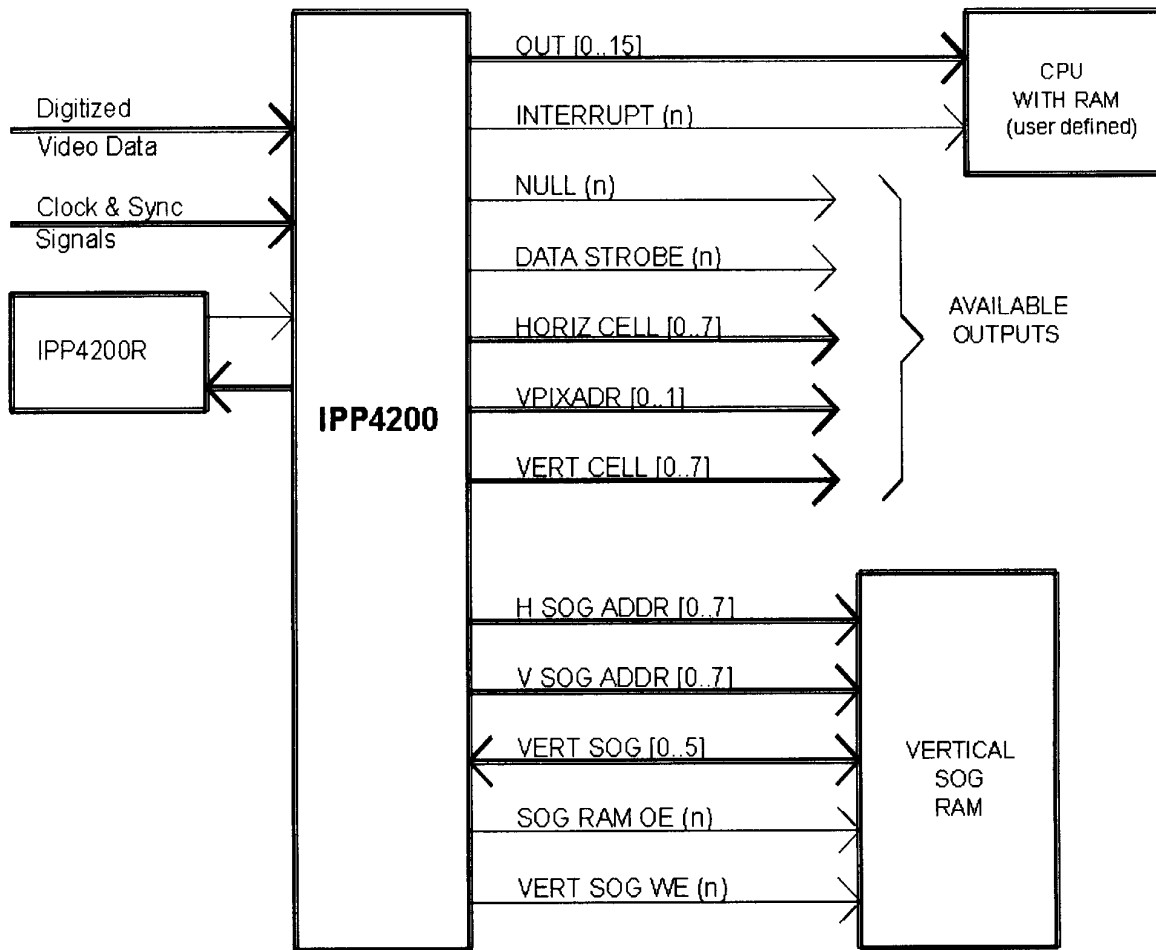
APPLICATIONS

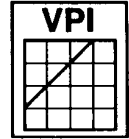
- Boundary Locator
- Object Identifier
- Object Orientation Detection
- Machine Vision Control, Robotics
- General Purpose Image Processing
- Conveyor Belt Processing/Handling



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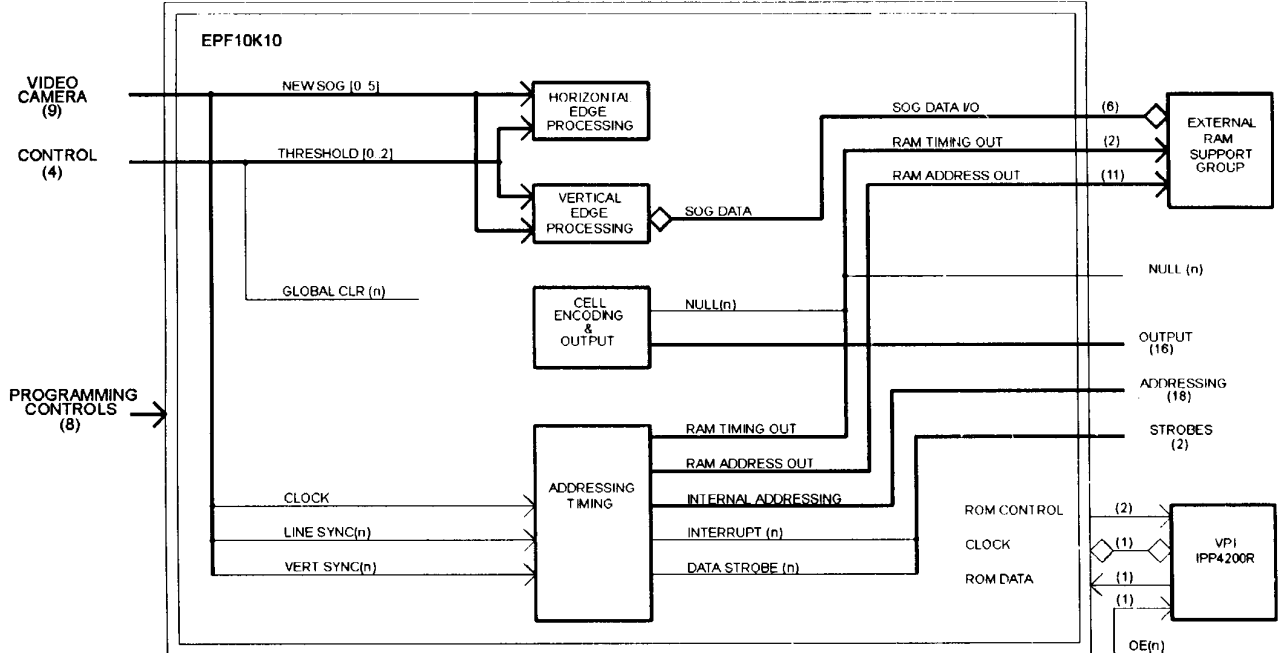
TYPICAL APPLICATION





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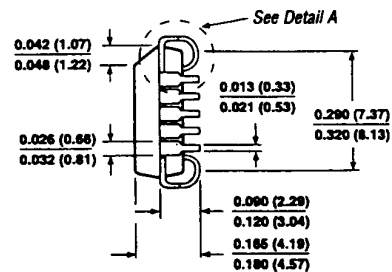
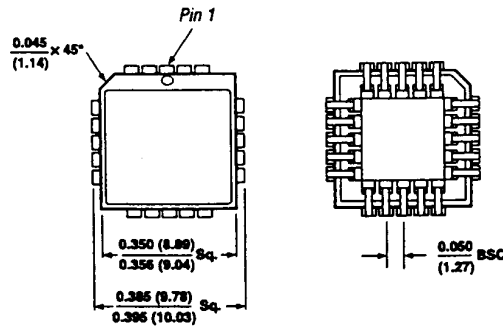
SIMPLIFIED BLOCK DIAGRAM



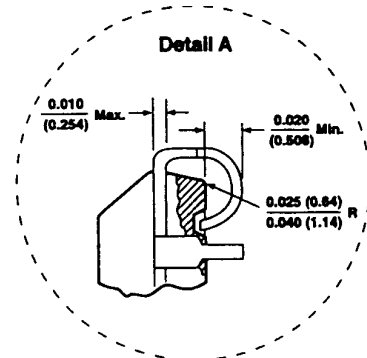
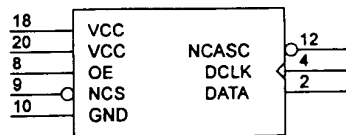
20-Pin Plastic J-Lead Chip Carrier (PLCC)

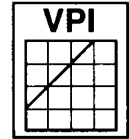
PACKAGE CONFIGURATION

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only.



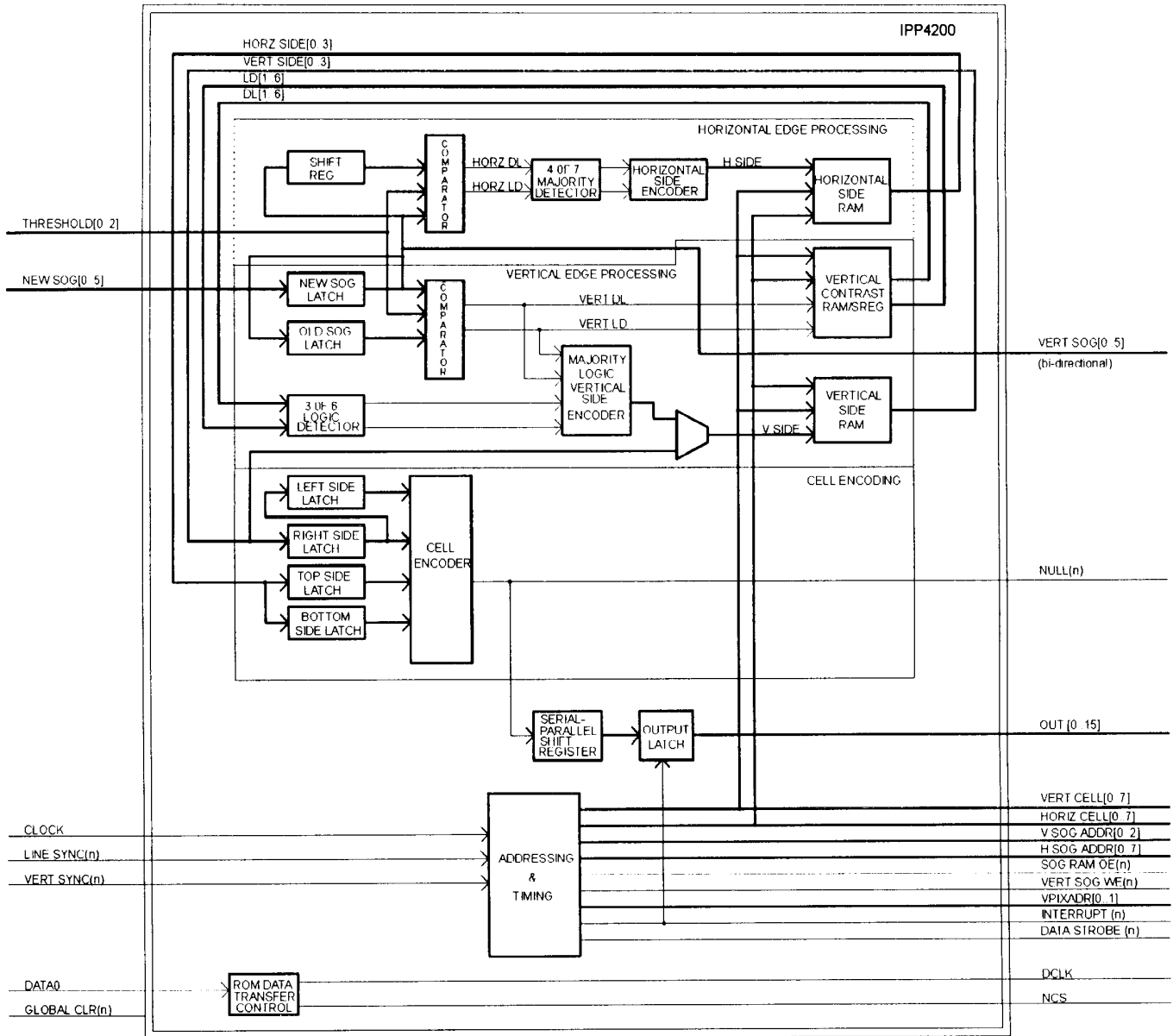
PIN-OUTS FOR THE IPP4200

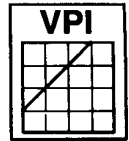




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FUNCTIONAL BLOCK DIAGRAM

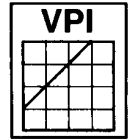




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Pin Assignment

PIN	SIGNAL NAME	TYPE	PIN	SIGNAL NAME	TYPE
79	CLOCK	Input	205	INTERRUPT (n)	Output
18	NEW SOG 0	Input	196	NULL (n)	Output
12	NEW SOG 1	Input	168	DATA STROBE (n)	Output
13	NEW SOG 2	Input	60	HORIZ CELL 0	Output
147	NEW SOG 3	Input	133	HORIZ CELL 1	Output
16	NEW SOG 4	Input	132	HORIZ CELL 2	Output
17	NEW SOG 5	Input	121	HORIZ CELL 3	Output
27	THRESHOLD 0	Input	172	HORIZ CELL 4	Output
29	THRESHOLD 1	Input	111	HORIZ CELL 5	Output
31	THRESHOLD 2	Input	112	HORIZ CELL 6	Output
80	GLOBAL CLR (n)	Input	158	HORIZ CELL 7	Output
183	LINE SYNC (n)	Input	45	VPIXADR 0	Output
78	VERT SYNC (n)	Input	134	VPIXADR 1	Output
154	nCE	Input	47	VERT CELL 0	Output
155	DCLK	Input	189	VERT CELL 1	Output
156	DATA0	Input	198	VERT CELL 2	Output
105	nCONFIG	Input	63	VERT CELL 3	Output
2	CONF DONE	I/O	61	VERT CELL 4	Output
52	nSTATUS	I/O	200	VERT CELL 5	Output
108	MSEL0	Input	207	VERT CELL 6	Output
107	MSEL1	Input	55	VERT CELL 7	Output
50	TMS	Input	162	H SOG ADDR 0	Output
1	TCK	Input	163	H SOG ADDR 1	Output
153	TDI	Input	164	H SOG ADDR 2	Output
4	TDO	Output	204	H SOG ADDR 3	Output
51	nTRST	Input	99	H SOG ADDR 4	Output
166	OUT 0	Output	120	H SOG ADDR 5	Output
88	OUT 1	Output	101	H SOG ADDR 6	Output
96	OUT 2	Output	161	H SOG ADDR 7	Output
97	OUT 3	Output	69	V SOG ADDR 0	Output
53	OUT 4	Output	70	V SOG ADDR 1	Output
206	OUT 5	Output	131	V SOG ADDR 2	Output
54	OUT 6	Output	149	VERT SOG 0	I/O
38	OUT 7	Output	11	VERT SOG 1	I/O
148	OUT 8	Output	19	VERT SOG 2	I/O
142	OUT 9	Output	10	VERT SOG 3	I/O
71	OUT 10	Output	144	VERT SOG 4	I/O
75	OUT 11	Output	150	VERT SOG 5	I/O
74	OUT 12	Output	208	SOG RAM OE (n)	Output
141	OUT 13	Output	192	VERT SOG WE (n)	Output
143	OUT 14	Output			
187	OUT 15	Output			



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SIGNAL DEFINITIONS

POWER&PROGRAMMINGPINS *(see appropriate Altera data sheets)*

The following power pins must be connected to VCC

VCCINT
6, 23, 35, 43, 76, 77, 106, 109, 117, 137, 145, 181

VCCIO
5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194

The following power return pins must be connected to ground.

GNDINT
21, 33, 49, 81, 82, 123, 129, 151, 185

GNDIO
20, 32, 48, 59, 72, 91, 124, 130, 152, 171, 188, 201

nCE, MSEL0, MSEL1, nTRST
These pins must be connected to ground.

nCONFIG, TMS, TCK, TDI
These pins must be connected to VCC.

DCLK
This pin must be connected to the DCLK pin of the IPP4200R. It provides the clock for data transfer from the IPP4200R to the PLD.

DATAO
This pin must be connected to the DATA pin of the IPP4200R. It provides data from the IPP4200R to the PLD.

nSTATUS
This pin must be connected to the OE (n) pin of the IPP4200R. It also must be connected to VCC through a 1K ohm resistor.

CONF DONE
This pin must be connected to the nCS pin of the IPP4200R. It also must be connected to VCC through a 1K resistor.

CLOCK & TIMING INPUTS

CLOCK
The pixel clock from the video camera supplies the clocking to the IPP. All input signals from the video camera transition on the positive going edge of CLOCK. The maximum clock rate is 25 MHz.

LINE SYNC (n)
This signal is supplied from the video camera. It controls the incrementing of the line counter with the IPP to control memory access addresses. It also terminates the pixel counter (for position within a horizontal line) of the IPP to permit adjustment to any line length within the IPP addressing limitations of 1024 pixels.

VERT SYNC (n)

This input is supplied from the video camera. It controls the reset of address counters within the IPP to the start of a new image trace. This is the vertical retrace signal for interlaced camera mode and is the frame sync for non-interlaced mode. This must be connected to VCC for linear array camera operation.

DATA INPUTS

NEWSOG [0..5]
These input data are the pixel shades-of-gray (SOG) light intensity data from a digital video camera. Bit 0 is the least significant bit (Isb). This input range should be over the dynamic range of the image for best results. Video cameras having resolution greater than six bits can utilize the greater resolution to translate the IPP input to the dynamic six bit range.

CONTROL INPUTS

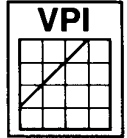
THRESHOLD [0..2]
These inputs provide control to the comparators of the horizontal and vertical edge processing to provide a differential threshold. This must be exceeded by the absolute difference of the two sample inputs of the comparator before contrast (DL or LD) is indicated. Bit 0 is the Isb. (See Table I and note I).

GLOBAL CLR (n)
This signal clears most of the internal latched elements when in the active low level. These internal latched elements will self initialize after a single Field of operation.

DATA&FLAG OUTPUTS AND I/O

VERTSOG [0..5]
These I/O are the SOG data from the video camera latched and routed by the IPP to RAM. The latched samples written to the RAM are every fourth pixel corresponding to the left most pixel position with the cell for the horizontal scan line. Bit 0 is the Isb. Signal VERT SOG WE (n) causes the loading of these data.

OUT [0..15]
These outputs are the NULL (n) status data for 16 consecutive cells in a horizontal row. The data are valid at the negative going edge of INTERRUPT (n) and are maintained until the next negative going edge. Bit 0 is the Isb; it represents the left-most cell of the 16 bit sequence.



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NULL (n)

This output signal indicates the boundary status of the currently accessed cell. It is a flag output for the cell being evaluated. A low level output defines a null status; a high level defines a boundary detection status of the cell. The data are valid at the negative going edge of DATA STROBE (n).

TIMING & CONTROL OUTPUTS

SOG RAM OE (n)

This timing signal enables the external Shades-Of-Gray RAM when in the active low level.

DATA STROBE (n)

This negative going pulse provides timing for external processing of the IPP output flag NULL (n). This may be latched on the negative going edge.

INTERRUPT (n)

This negative going pulse provides timing for external processing of the IPP output OUT [0..15]. It is expected to be used to signal an external processor to load the available data.

VERT SOG WE (n)

IPP output data VERT SOG [0..5] are written to external RAM during the low interval of this signal.

ADDRESS OUTPUTS

HORIZCELL [0..7]

These data are the low order horizontal cell address. They can be used to assist the external processor in directing OUT [0..15] data to RAM.

VERT CELL [0..7]

These data are the high order vertical cell address. They can be used to assist the external processor in directing OUT [0..15] data to RAM.

VPIXADR [0..11]

These address outputs define the current vertical line address within a cell. Bit 0 is the lsb. Data OUT [0..15] is available only when this address is 3.

H SOG ADDR [0..7]

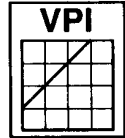
These data are the low order address inputs to the external RAM device storing IPP output data VERT SOG [0..5]. Bit 0 is the lsb.

V SOG ADDR [0..2]

These data are the high order address inputs to the external RAM device storing IPP output data VERT SOG [0..5]. Bit 0 is the lsb.

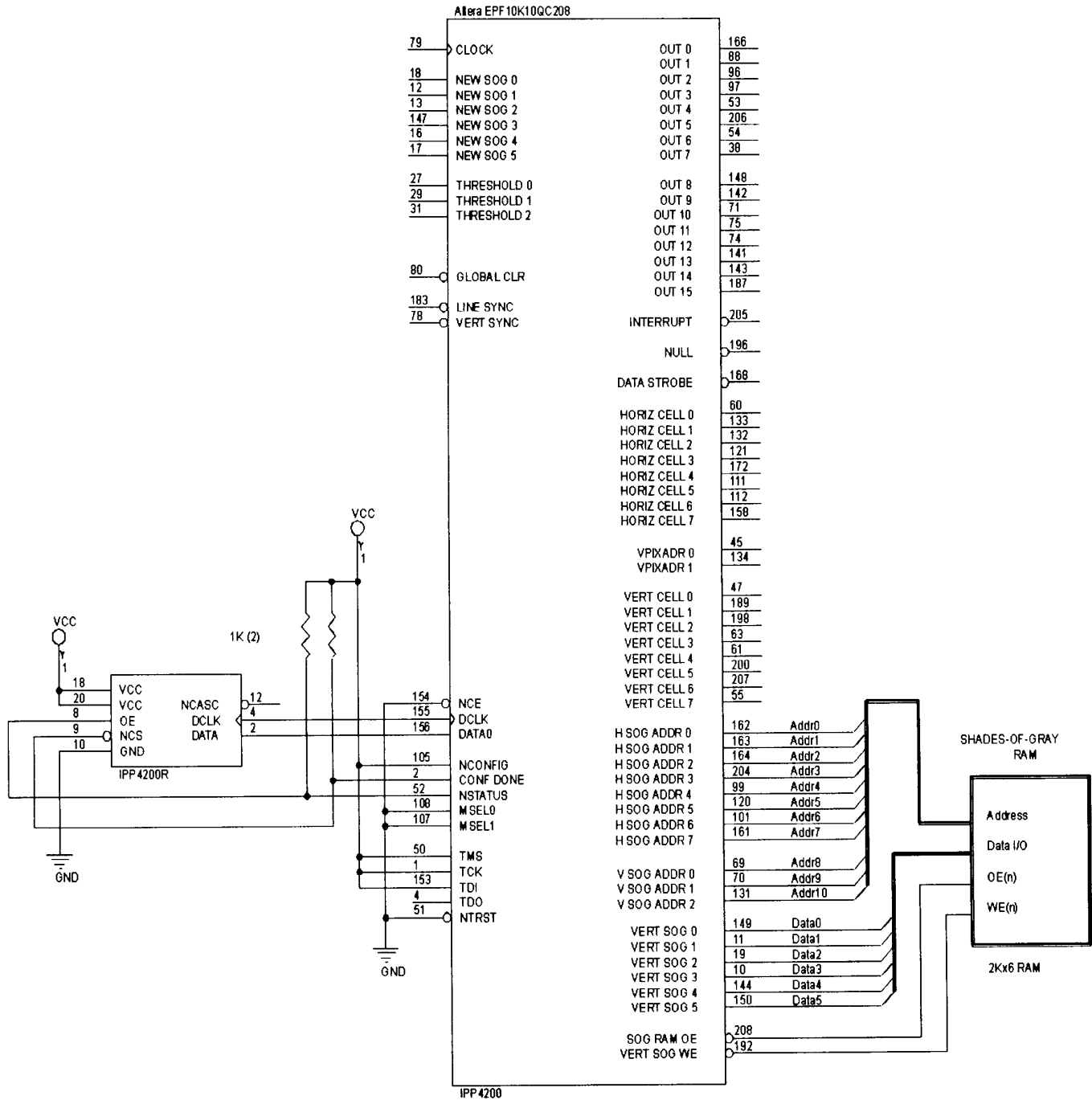
Note I.

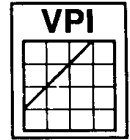
This input can be dynamically changed asynchronously; the resultant change will be initiated synchronously with the start of an image field.



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Figure1 Block Diagram of IPP Connected to External Support RAM Group





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DESIGN IMPLEMENTATION

The IPP4200 function is implemented in an Altera EPF10K10QC208 Programmable Logic Device (PLD). IPP4200R is the designation for the Video Perception, Inc. Read-Only-Memory (ROM) device used to load the Altera PLD each time power is applied to the circuit. The operating PLD-ROM pair is hereafter designated an IPP4200.

GENERAL INFORMATION

The IPP4200, hereafter referred to as Image Pre-Processor (IPP), is a real time image processor which translates digital pixel data, received in the horizontal scanning pattern as transmitted by a video camera, into an encoded form optimized for computer follow-on processing. It processes the horizontal scanned data to determine horizontal edge conditions. It controls the storing of vertical columns of pixel data to perform a pseudo scan in the vertical direction. It then determines vertical edge conditions. The edge data derived by horizontal and vertical edge processing are stored in RAM until all needed components of these data are available for encoding. It then retrieves these components to generate status data. Status data from several regions are collected into a common output before strobing an external device to inform it that these are available. Address and timing is developed internally to control the external support RAM. Figure 1 is a block diagram of the IPP connected to the external support RAM.

CELL STRUCTURE AND PROCESSING OVERVIEW

The IPP sub-divides the image viewing area into 4x4 pixel space regions called cells (see Figure 2). These cells are bounded by lines which sub-divide the image viewing area every four pixel spaces in both the horizontal and the vertical directions. The lines are along perimeter sides of these cells establishing 64K cells. The image is scanned in the horizontal direction by the natural scanning of the video camera along the perimeter sides of cells to detect edges in accordance with an algorithm to be defined later. Digitized pixel data (occurring along the vertical perimeter sides of cells) are accumulated in external RAM storage and pseudo scanned in the vertical direction in accordance with the same algorithm used in the horizontal direction.

Each cell shares sides with the adjacent cells creating 5x5 pixel cell matrices (at 4x4 pixel spaces). Figure 3 illustrates this structure. The horizontally detected edge status and the pseudo scanned vertically detected edge status, for each of the four sides, are each encoded to determine the cell status (single bit). The four encoded sides are then applied to a cell boundary encoder that encodes the resulting NULL (n) (see Figure 4). These data are valid at the negative going edge of DATA STROBE(n). The IPP controls the RAM storage of in-process data (to be used at a later interval); it retrieves these data at the proper timing as needed. The internal RAM used for development of vertical data requires eight horizontal scan lines of storage.

The internal RAM used for development of horizontal data requires only four horizontal scan lines storage. This RAM is re-used for follow-on scan lines; this technique requires relatively small memory storage space. The IPP responses to input control THRESHOLD is defined in Table I.

EDGE DETECTION

Edge detection is a multi-step process. The first step, in both the horizontal and vertical edge processing of Shades-Of-Gray (SOG) digitized pixel data, is to sequentially compare two pixels spaced seven spaces apart. This comparison of two samples is repeated each time the comparison-selection increments one pixel in the direction of scan.

A contrast indication, either DL or LD, is registered when the difference value of the two pixels of the sample exceed the absolute value of a differential threshold resulting from external control. The second step is to evaluate both the DL and the LD contrast indications with a four of seven majority logic circuit to determine edge locations. At the first occurrence of this majority, a location of the edge and the contrast type are registered. At the same time, the history of contrast indications is reset to assure that the frequency of edge indications will only be once per cell. The majority logic circuit filters image noise input; it also enhances edge detection. The third step is to encode the cell side status. The fourth step is to store the side status into internal RAM until data from other sides of the cell are available.

CELL ENCODING & DECODING

Cell encoding utilizes status from the four sides and position E (see Figures 4 and 5) to develop encoded boundary data. Because of the shared perimeter pixels of a cell with adjacent cells, linkage to adjacent cells is easily achieved during the decoding process. An example of the data generated as a result of an object in the viewing area is shown in Figure 6.

DATA TRANSFER TIMING

Data are placed in internal storage until the proper timing to retrieve them for use in the processing. The output data (OUT [0..15]) are the result of serial-to-parallel conversion of the NULL (n) data. Sixteen sequentially developed NULL (n) status data for cells in a horizontal row (see Figure 7) are made available to an external latch after the notification timing of the INTERRUPT (n) signal. Figures 8, 9, and 10 are timing diagrams of the output data development occurring only on cell line number 3.

