VIDEO PERCEPTION INCORPORATED

IPP4000R

CMOS Real Time Image Pre-Processor

25 MHz

The IPP4000R is a uniquely programmed device which when coupled with an Altera 10K10 PLD (user supplied identified as IPP4000) supports image processing and motion detection. It is ideally suited to video camera based operation because it can substantially reduce the band width of data transmitted from the camera. It translates a digitized video image into an encoded set of tangent line segments with inherent image noise filtering and image enhancement. It can also develop encoded texture data. These encoded data are in substantially condensed form and are intended as input data to a computer. The form of the encoded data tangent line segments is ideally suited for linkage and evaluation by the computer. The IPP4000 can be externally controlled to change a differential threshold level, a motion alarm tolerance level, and the mode (boundary vs. texture); these can be changed asychronously with synchronized changes occurring the next frame. Motion data are characterized in very condensed form while providing a great degree of discrimination. The IPP4000 processes digitized video camera data in real time with minimal data storage to RAM. It supports a maximum image horizontal line size of 1024 pixels while self-adjusting to any shorter line. There are no size limitations in the vertical direction (for non-motion detection applications) permitting it to be used for both linear array and two dimension video cameras. The maximum vertical size for motion detection is 1024 lines per field (2048 lines per frame for interlaced cameras). Multiple IPP4000 devices can be cascaded and/or used for dual (or more) differential threshold processing with internally integrated handshake lines. Image resolution is supported by a 25 MHz (preliminary) pixel clock rate. Image processing and motion detection are processed concurrently. A high resolution mask is supported which permits masking of image areas from motion detection.

FEATURES

- **Operates at 25 MHz Clock** Rate
- Proddes Real Time Image **Processing**
- Proddes Discriminating **Motion Detection**
- Translates Images **to** Condensed Form for PC
- **Encodes Image Tangent Line Segment** Boundary
- Supports Computer Boundary Linkage
- Supports Rate of Angular Boundary Change **Evaluation**
- **Encodes Image Texture**
- **Filter Image Noise**
- **Enhances Image Boundary**
- **Provides up to 1024 x 1024 Processing Resolution**
- Supports **Cascadeable Operation to Unlimited Resolution**
- Supports Both Linear Array **and Two Dimension Video Cameras**
- **Overcomes Computer Bus Overload**
- Supports Camera-Based or External-to-Computer **Usage**
- Supports Dynamic Differential **Threshold Adjustmere**
- Supports Dual Differential **Threshold Processing**
- Supports **Dynamic Motion Tolerance Adjustmere**
- Supports Dynamic Boundary/Texture Mode Change
- Supports Concurrent Image **Processing and Motion Detection**
- Supports Masking **for Motion Detection**

APPLICATIONS

- **Machine Vision Control,** Robotics
- **Intrusion Detection/Object Recognition**
- **Airport Flight Safety**
- General Purpose Image **Processing**
- **Conveyor Belt** Processing/Handling
- Line Boundary Archive Encoding
- **Image Motion Data Compression**
- Artifical **Intelligence**
- Military Perimeter Security
- Image Recognition
- **Auto Speed Molter**
- 3-Dimensional Image **Processing**
- **Intrusion DetectionObject** Recognition
- Dollar Bill Chargers/Sorters
- Line Drawingg Encoder/Reader
- Handwriting /Signature Anaylsis
- **Texture** AllayIsis
- Bar Code/Matrix Code Readers
- **Missile** Recognition/Guidance
- Military Aircraft Fatemy **Threat Detection**
- Visual/Ultra Violet/Infra-Red/Laser/Magnetic/ Radar/X-Ray/Ultra- Sonic Operating Source **Scarenet Systems**

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U.S. Patent # 4,897,719

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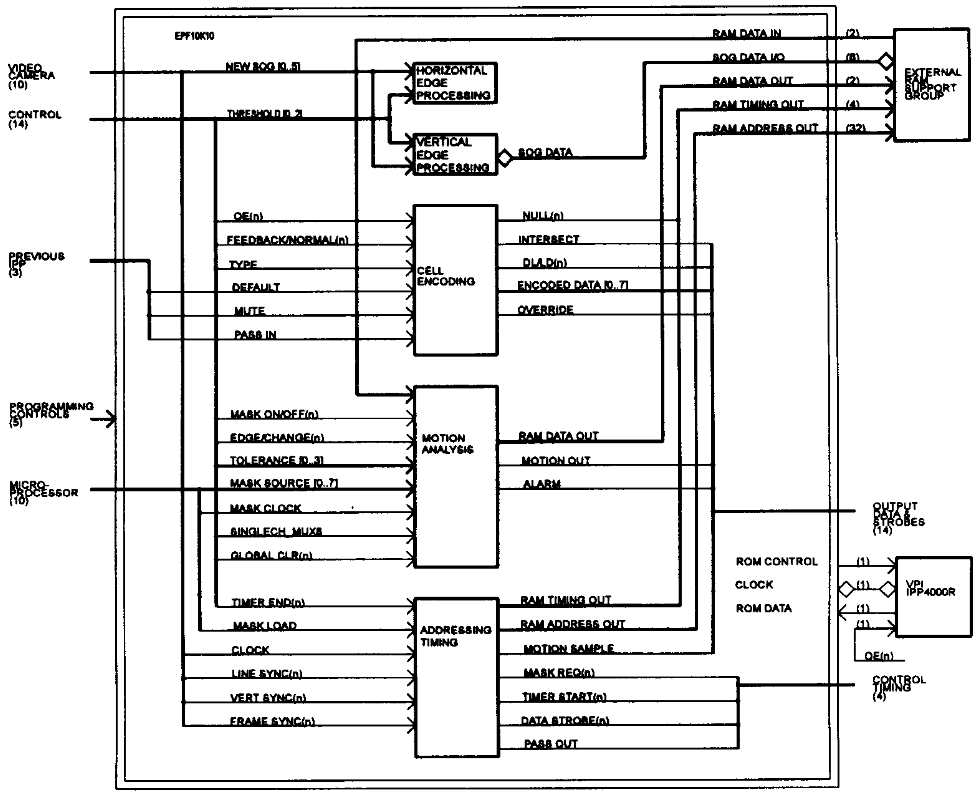
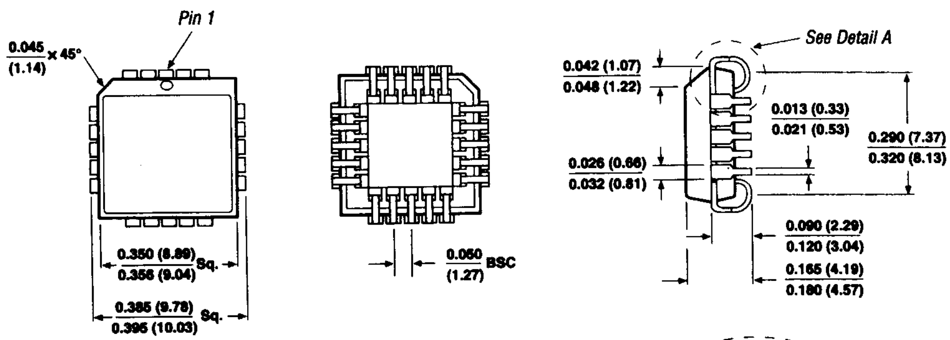
Simplified Block Diagram

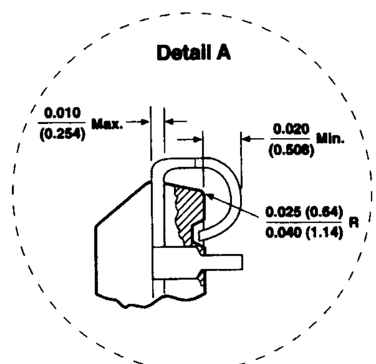


20-Pin Plastic J-Lead Chip Carrier (PLCC)

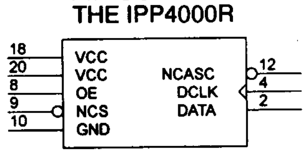
PACKAGE CONFIGURATION

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only.





PIN-OUTS FOR THE IPP4000R



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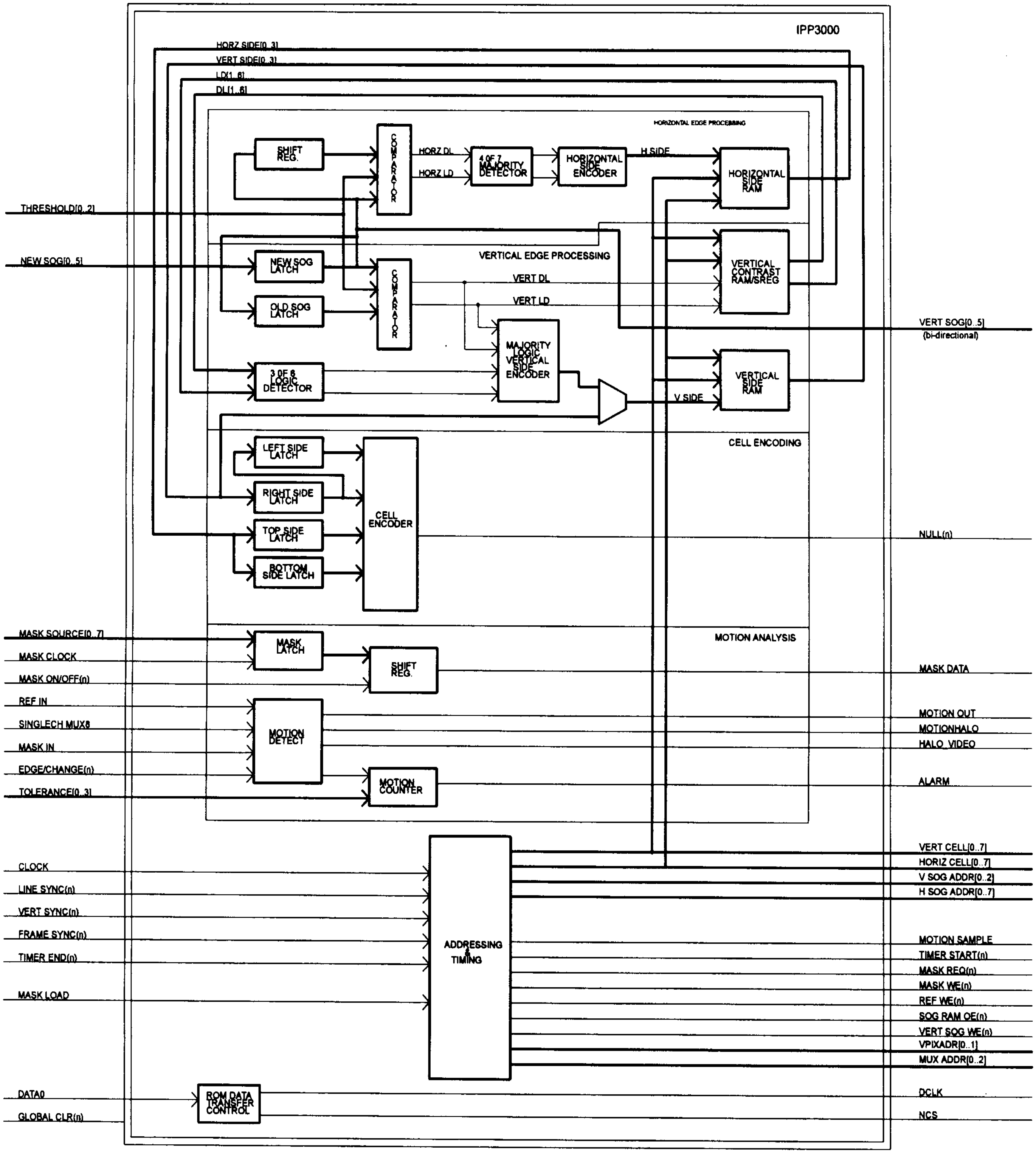
Functional Block Diagram



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Pin Assignment

(of Altera EPF10K10QC208 when configured as an IPP4000)

PIN	SIGNAL NAME	TYPE	PIN	SIGNAL NAME	TYPE
128	TIMER END(n)	Input	67	TIMER START(n)	Output
79	CLOCK	Input	92	PASS OUT	Output
18	NEW SOG 0	Input	80	OVER RIDE	Tri
12	NEW SOG 1	Input	44	INTERSECT	Tri
13	NEW SOG 2	Input	166	ENCODED DATA 0	Tri
147	NEW SOG 3	Input	88	ENCODED DATA 1	Tri
16	NEW SOG 4	Input	96	ENCODED DATA 2	Tri
17	NEW SOG 5	Input	97	ENCODED DATA 3	Tri
27	THRESHOLD 0	Input	53	ENCODED DATA 4	Tri
29	THRESHOLD 1	Input	206	ENCODED DATA 5	Tri
31	THRESHOLD 2	Input	54	ENCODED DATA 6	Tri
135	TOLERANCE 0	Input	38	ENCODED DATA 7	Tri
30	TOLERANCE I	Input	168	DATA STROBE(n)	Tri
157	TOLERANCE 2	Input	45	VPIXADR 0	Output
136	TOLERANCE 3	Input	134	VPIXADR 1	Output
28	TYPE	Input	162	H SOG ADDR 0	Output
41	EDGE/CHANGE(n)	Input	163	H SOG ADDR 1	Output
39	FEEDBACK/NORMAL(n)	Input	164	H SOG ADDR 2	Output
24	SINGLECH/MUX8(n)	Input	204	H SOG ADDR 3	Output
26	DE(n)	Input	99	H SOG ADDR 4	Output
191	DEFAULT	Input	120	H SOG ADDR 5	Output
182	MUTE	Input	101	H SOG ADDR 6	Output
25	PASS IN	Input	161	H SOG ADDR 7	Output
148	MASK SOURCE 0	Input	69	V SOG ADDR 0	Output
142	MASK SOURCE I	Input	70	V SOG ADDR 1	Output
71	MASK SOURCE 2	Input	131	V SOG ADDR 2	Output
75	MASK SOURCE 3	Input	149	VERT SOG 0	I/O
74	MASK SOURCE 4	Input	11	VERT SOG 1	I/O
141	MASK SOURCE 5	Input	19	VERT SOG 2	I/O
143	MASK SOURCE 6	Input	10	VERT SOG 3	I/O
187	MASK SOURCE 7	Input	144	VERT SOG 4	I/O
184	MASK CLOCK	Input	150	VERT SOG 5	I/O
186	MASK LOAD	Input	208	SOG RAM OE(n)	Output
73	MASK ON/OFF(n)	Input	192	VERT SOG WE(n)	Output
40	MASK IN	Input	60	HORIZ CELL 0	Output
119	REF IN	Input	133	HORIZ CELL 1	Output
80	GLOBAL CLR(n)	Input	132	HORIZ CELL 2	Output
183	LINE SYNC(n)	Input	121	HORIZ CELL 3	Output
78	VERT SYNC(n)	Input	172	HORIZ CELL 4	Output
127	FRAME SYNC(n)	Input	111	HORIZ CELL 5	Output
154	nCE	Input	112	HORIZ CELL 6	Output
155	DCLK	Input	158	HORIZ CELL 7	Output
156	DATA0	Input	47	VERT CELL 0	Output
105	nCONFIG	Input	189	VERT CELL 1	Output
108	MSEL0	Input	198	VERT CELL 2	Output
107	MSEL1	Input	63	VERT CELL 3	Output
2	CONF_DONE	I/O	61	VERT CELL 4	Output
52	nSTATUS	I/O	200	VERT CELL 5	Output
50	TMS	Input	207	VERT CELL 6	Output
1	TCK	Input	55	VERT CELL 7	Output
153	TDI	Input	62	MUX ADDR 0	Output
4	TDO	Output	199	MUX ADDR 1	Output
51	nTRST	Input	46	MUX ADDR 2	Output
			68	MASK DATA	Output
			196	NULL(n)	Output
			197	MASK WE(n)	Output
			104	REF WE(n)	Output
			115	MOTION OUT	Output
			205	MOTION SAMPLE	Output
			169	ALARM	Output
			116	MASK REQ(n)	Output
			175	MOTION HALO	Output
			122	HALO VIDEO	Output

NOTE: Refer to the Altera EPF10K10QC208 data sheets for power and ground connections.

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SIGNAL DEFINITIONS

POWER & PROGRAMMING PINS (see appropriate Altera data sheets)

The following power pins must be connected to VCC

VCCINT

6, 23, 35, 43, 76, 77 106, 109, 117, 137, 145, 181

VCCIO

5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194

The following power return pins must be connected to ground.

GNDINT

21, 33, 49, 81, 82, 123, 129, 151,185

GNDIO

20, 32, 48, 59, 72, 91,124, 130, 152, 171, 188, 201

nCE, MSELO, MSEL1, nTRST

These pins must be connected to ground.

nCONFIG, TMS, TCK, TDI

These pins must be connected to VCC.

DCLK

This pin must be connected to the DCLK pin of the IPP4000R. It provides the clock for data transfer from the IPP4000R to the PLD.

DATA0

This pin must be connected to the DATA pin of the IPP4000R. It provides data from the IPP4000R to the PLD.

nSTATUS

This pin must be connected to the OE (n) pin of the IPP4000R. It also must be connected to VCC through a 1K ohm resistor.

CONF DONE

This pin must be connected to the nCS pin of the IPP4000R. It also must be connected to VCC through a 1K resistor.

CLOCK & TIMING INPUTS

CLOCK

The pixel clock from the video camera supplies the clocking to the IPP. All input signals from the video camera transition on the positive going edge of CLOCK. The maximum clock rate is 25 MHz.

LINE SYNC (n)

This signal is supplied from the video camera. It controls the incrementing of the line counter within the IPP to control memory access addresses. It also terminates the pixel counter (for position within a horizontal line) of the IPP to permit adjustment to any line length within the IPP addressing limitations of 1024 pixels. This can be extended with cascaded operation.

VERT SYNC (n)

This input is supplied from the video camera. It controls the reset of address counters within the IPP to the start of a new image trace. This is the vertical retrace signal for interlaced camera mode and is the frame sync for non-interlaced mode. This must be connected to VCC for linear array camera operation.

FRAME SYNC (n)

Only interlaced mode camera operation utilizes this input; it must be connected to VCC for non-interlaced or linear array camera operation. This signal synchronizes the internal IPP counters to the video camera when employed.

MASK CLOCK

An external microprocessor supplies this clock during read operations from an external RAM (see Figure l) to strobe the data being read from the RAM. These data are also latched by the IPP.

TIMER END (n)

When the timing of reference field storage update is controlled by an external timer, the negative going edge of the timer output initiates the synchronous loading of the IPP support Reference RAM at the start of a vertical retrace. This initiation signal may be asychronous. This loads the current image null status data (1 bit per cell) into the Reference RAM. The loading can be initiated by any other external control operation causing a negative going transition of this signal.

DATA INPUTS

NEW SOG [0..5]

These input data are the pixel shades-of-gray (SOG) light intensity data from a digital video camera. Bit 0 is the least significant bit (lsb). This input range should be over the dynamic range of the image for best results. Video cameras having resolution greater than six bits can utilize the greater resolution to translate the IPP input to the dynamic six bit range.

REF IN

This input signal provides the null status of the current cell being internally addressed by the IPP from the data stored in the Reference RAM. A low state define a null status; a high state identifies a boundary condition. If a Reference RAM is not used, this input must be connected to either VCC or GND.

MASK IN

This input provides the mask status, of the current cell being internally addressed by the IPP, from the data stored in the Mask RAM. A low state defines a non-masked condition; a high state causes any motion indication to be ignored for that cell. If a Mask RAM is not used, this input must be connected to VCC to disable motion detection or it must be connected to

GND to enable motion detection if a Reference RAM is being used.

MASK SOURCE [0..7]

Mask data is supplied to the IPP by these inputs and is strobed by signal MASK CLOCK. Bit 0 is the lsb.

CONTROL INPUTS

THRESHOLD [0..2]

These inputs provide control to the comparators of the horizontal and vertical edge processing to provide a differential threshold. This must be exceeded by the absolute difference of the two sample inputs of the comparator before contrast (DL or LD) is indicated. Bit 0 is the lsb. (See Table III and note 1).

TOLERANCE [0..3]

These inputs provide preload control to counters of the motion detector of the IPP. This provides a required count of the cells containing motion indications before an alarm status is indicated. Bit 0 is the lsb. (See.Table II and note 1).

FEEDBACK/NORMAL (n)

The user can select from two modes of data encoding when there are edge indications of three or more sides. In the NORMAL (low) selection mode, three side data are supplied with an individual code for each combination of three sides. Four side indications are encoded with single INTERSECT code. In the FEEDBACK (high) selection mode, all three or more side conditions are encoded with the single INTERSECT code. A count of the density of INTERSECT codes within the image area of interest provides feedback to the controller for optimum THRESHOLD setting. When the threshold is set to low, there will be an excessive number of INTERSECT code indications.

OE (n)

Selected outputs (see note 2) are placed in the tri-state condition when this signal is high; when the signal is low, these outputs are active except as defined by note 2.

EDGE/CHANGE (n)

This input selects one of two modes of motion detection when the cell being monitored is not masked. In the CHANGE (low) mode, a motion cell count is detected if the current NULL (n) output indication does not match that provided by the REF IN input. In the EDGE (high) mode, a motion cell count is detected if the REF IN input is low and the NULL (n) output indication is high.

MASK ON/OFF (n)

In the OFF (low) mode of this input, there is no masking of data to the motion detector. In the ON (high) mode, the motion counter input is disabled from detecting additional counts where masked.

MASK LOAD

This signal initiates the conversion and loading of a field of MASK SOURCE [0..7] data (in eight bit format) to MASK DATA at the IPP output to the Mask RAM in single bit format. The loading process is synchronous with the image field address timing; the MASK LOAD input may be applied asychronously. Mask RAM loading is initiated as a result of a high input.

SINGLECH/MUX8 (n)

The user can select from multiplexed or non-multiplexed motion detection operation. Single channel operation is selected with the signal in the high level. Comparisons of image boundary conditions are made on every other field. Multiplexed operation of eight channels is selected with the signal low. Comparisons of image boundary conditions are made on every field.

GLOBAL CLR (n)

The signal clears most of the internal latched elements when in the active low level. These internal latched elements will self initialize after a single field of operation.

IPP INTERFACE INPUTS (SeeTableIV)

DEFAULT

The DEFAULT input defines the major/minor threshold role when two IPP devices are connected in a dual threshold processing mode. Table IV defines when the selected IPP outputs listed in note 2 are active and when they are tri-state. When operating with a single IPP, connect this input to VCC.

MUTE

When this input is high, the selected IPP outputs listed in note 2 are tri-state.

PASS IN

When this input is low, the selected IPP outputs listed in note 2 are tri-state.

DATA & FLAG OUTPUTS AND I/O

VERY SOG [0..5]

These I/O are the SOG data from the video camera latched and routed by the IPP to RAM. The latched samples written to the RAM are every fourth pixel corresponding to the left most pixel position within the cell for the horizontal scan line. Bit 0 is the lsb. Signal VERY SOG WE (n) causes the loading of these data.

ENCODED DATA [0..7]

These outputs are encoded data result for the cell. The data are valid at the negative going edge of DATA STROBE (n). Bit 0 is the lsb.

NULL (n)

This output signal indicates the boundary status of the Currently accessed cell. It is a flag which is also used as data to the Reference RAM during a single field update; the frequency of this update is controlled by the TIMER END (n) input. Signal REF WE (n) causes the loading of this signal. A low level output defines a null status; a high level defines a boundary detection status of the cell. The data are valid at the negative going edge of DATA STROBE (n).

INTERSECT

Depending upon the selection mode, this output signal is a flag to indicate the presence of edge detection at more than two sides or more than three sides. The output response is under control of input FEEDBACK/ NORMAL (n) (see the description for this signal). A low level indicates there is no intersect condition; a high level indicates there is intersect condition. The.data are valid at the negative going edge of DATA STROBE (n).

MASK DATA

This output signal is valid only during the single field of Mask RAM update initiated by the MASK LOAD input. Signal MASK WE (n) causes the loading of this signal. A high level indicates a masked condition for the accessed cell: a low level permits motion detection counting for the cell.

MOTION OUT

This output signal provides the motion status for the current accessed cell. A high level is a motion count; a low level is no indication of motion.

ALARM

This signal is a flag indicating the presence of motion in excess of that controlled by the TOLERANCE [0..3] inputs. The flag goes high if the motion count exceeds that defined by Table II; otherwise, it remains low. The flag indication remains active from the time of first detection of motion until the time that motion ceases.

MOTIONHALO

This output signal provides motion data representative of cell status. It also provides a halo around objects in motion when multiplexed with the analog video under control of signal HALO VIDEO (n). The video coax cable can be used to transmit motion data to a central location. The data can easily be removed from the multiplexed signal for further computer motion analysis.

TIMING & CONTROL OUTPUTS

SOG RAM OE (n)

This timing signal enables the external Shades-Of-Gray RAM when in the active low level.

HALO VIDEO (n)

This signal controls the multiplexed selection of either digital motion data or analog video data through an external analog multiplexer. The digital data are output at MOTIONHALO.

OVER RIDE

This signal is used to take output control from another IPP used in a dual threshold operating configuration (two IPP devices); this occurs when its input THRESHOLD[0..2] setting is the greater of the two, when its DEFAULT input is low, and when it has detected a boundary condition. It goes high during these conditions to set the other IPP to tri-state output conditions.

PASS OUT

This signal goes high when the internal horizontal line pixel position counter of the IPP is equal to or greater than 1008. This output signal is used when another IPP device is cascaded; the PASS OUT signal is connected to the PASS IN input signal of the following IPP to cause it to start processing. This provides a 16 pixel overlap needed for the following IPP to develop history; this assures a continuous flow of output encoding across IPP boundarys.

TIMER START (n)

This signal is a negative going pulse (when active) to initiate an external timing device to begin a new timing interval. The external timer provides the TIMER END (n) (low) input signal to the IPP at the completion of the timing interval. This low TIMER END (n) input causes the TIMER START (n) output to go low; consequently, this is a continuous process causing update of the Reference RAM data with a field of the current NULL (n) data on each occurrence.

MASK REQ (n)

This signal is a negative going pulse used to signal an external microprocessor (loading mask data) that the IPP is ready for another byte of mask data. It is used to synchronize the loading of mask data during a single image field.

DATA STROBE (n)

This negative going pulse provides timing for external processing of the IPP output data ENCODED DATA [0..7] and IPP output flags NULL (n) and INTERSECT. These may be latch on the negative going edge.

MOTION SAMPLE

This positive going pulse provides timing for external processing of the IPP output MOTION OUT. This output may be latched on the positive going edge or during the high interval.

MASK WE (n)
IPP output MASK DATA are written to external RAM during the low interval of this signal.

REF WE (n)
IPP output NULL (n) data are written to external RAM during the low interval of this signal.

VERT SOG WE (n)
IPP output VERT SOG [0..5] data are written to external RAM during the low interval of this signal.

ADDRESS OUTPUTS

HORIZ CELL [0..7]
These data are the low order address inputs to the external RAM devices storing IPP output data NULL (n) and MASKDATA. Bit 0 is the lsb.

VERT CELL [0..7]
These data are the high order address inputs to the external RAM devices storing IPP outputs NULL (n) and MASK DATA. Bit 0 is the lsb.

H SOG ADDR [0..7]
These data are the low order address inputs to the external RAM device storing IPP output data VERTSOG [0..5]. Bit 0 is the Isb.

V SOG ADDR [0..2]
These data are the high order address inputs to the external RAM device storing IPP output data VERTSOG [0..5]. Bit 0 is the Isb.

VPIXADR [0..1]
These address outputs define the current vertical line address within a cell. Bit 0 is the lsb.

MUX ADDR [0..2]
These address outputs are field count. They determine the high order address applied to the external Reference RAM and Mask RAM. They can also be used to control the selection of an external video multiplexer.

Note 1.
The input can be dynamically changed asychronously; the resultant change will be initiated synchronously with the start of an image field.

Note 2.
Signals which go tri-state, when selected, are ENCODED DATA [0..7], INTERSECT, DATA STROBE (n), and OVER RIDE. These also go tri-state during the first eight horizontal lines of a field and the first 16 pixels of each horizontal line. These data are not valid during these locations. These data are active on only every fourth horizontal line beginning at the 12th line (line number 11) unless other conditions cause them to go tri-state. These outputs also go tri-state when the internal pixel address of a horizontal line exceeds 1024; this results in a PASS OUT output status. Input signals OE (n), DEFAULT, MUTE and PASS IN also control the tri-state status of these outputs.

DESIGN IMPLEMENTATION

The IPP4000 function is implemented in an Altera EPF1OK10QC208 Programmable Logic Device (PLD). IPP4000R is the designation for the Video Perception, Inc. Read-Only-Memory (ROM) device used to load the Altera PLD each time power is applied to the circuit. The operating PLD-ROM pair is hereafter designated an IPP4000.

GENERAL INFORMATION

The IPP4000, hereafter referred to as Image Pre-Processor (IPP), is a real time image processor which translates digital pixel data, received in the horizontal scanning pattern as transmitted by a video camera, into an encoded form optimized for computer follow-on processing. It processes the horizontal scanned data to determine horizontal edge conditions. It controls the storing of vertical columns of pixel data to perform a pseudo scan in the vertical direction. It then determines vertical edge conditions. The edge data derived by horizontal and vertical edge processing are stored in RAM until all needed components of these data are available for encoding. It then retrieves these components to generate encoded data. It also processes texture during the horizontal edge processing to provide encoded texture data. Mask data can be loaded into the support group RAM under control of the IPP and an external microprocessor (see Figure 1). Reference data can be loaded into the support group RAM through timer initiation of the IPP control. The mask data disables motion detection over a selection of the many regions of the image called cells. A motion counter detects motion indications of comparisons of stored and real time image data representations of these cells of the image (when not masked). This provides a count of the difference indications. A motion tolerance can be input to the IPP to establish a motion count level that will cause an alarm. When that count per field is exceeded, the alarm flag will be set. Address and timing is developed internally to control the external support group RAM and to control handshake lines for multiple IPP operation. Figure 2 is a block diagram of the IPP connected to the external support group RAM. It illustrates the interface to the three basic RAM sections.

CELL STRUCTURE AND PROCESSING OVERVIEW

The IPP sub-divides the image viewing area into 4x4 pixel space regions called cells (see Figure 3). These cells are bounded by lines which sub-divide the image viewing area every four pixel spaces in both the horizontal and the vertical directions. The lines are along perimeter sides of these cells establishing 64K cells. The image is scanned in the horizontal direction by the natural scanning of the video camera along the perimeter sides of cells to detect edges in accordance with an algorithm to be defined later. Digitized pixel data occurring along the vertical perimeter sides of cells are accumulated in external RAM storage and pseudo scanned in the vertical direction in accordance with the same algorithm used in the horizontal direction.

Each cell shares sides with the adjacent cells creating 5x5 pixel cell matrices (at 4x4 pixel spaces). Figure 4 illustrates this structure. The horizontally detected edge locations and the pseudo scanned vertically detected edge locations, for each of the four sides, are each encoded into four bit data. One bit is a flag denoting the True/false status of edge detection at the side. One bit defines dark-to-light (DL) or light-to-dark (LD) light intensity transition status of that side at the detected edge. The remaining two bits define the position within the side (0 to 3) of the detected edge.

Providing boundary data are selected, the four encoded sides are then applied to a cell boundary encoder which encodes the resulting ENCODED DATA (see Figure 5). A unique code is provided for all combinations having one, two and three sides with edge detection. Different codes are assigned, to combinations having two side edge detection, for DL and LD cell encoding. An intersect code status develops when four sides have an edge indication. If none of the sides has an edge indication, a null code is assigned.

Flags INTERSECT and NULL(n) are output when the ENCODED DATA are valid. These data are valid at the negative going edge of DATA STROBE(n). If texture data are selected, a different algorithm generates ENCODED DATA representing texture. The four least significant bits of ENCODED DATA provide the frequency of occurrences of contrast detection in the horizontal scan direction over a window of three cells centered on the cell being monitored.

The IPP controls the RAM storage of in-process data developed to be used at a later interval; it retrieves these data at the proper timing as needed. The internal RAM used for development of vertical data requires eight horizontal scan lines of storage. The internal RAM used for development of horizontal data requires only four horizontal scan lines storage. This RAM is reused for follow-on scan lines; this technique requires relatively small memory storage space. The IPP responses to input controls TOLERANCE, THRESHOLD, DEFAULT, MUTE and PASS IN are defined in Table I, Table II and Table III.

EDGE DETECTION

Edge detection is a multi-step process. The first step, in both the horizontal and vertical edge processing of Shades-Of-Gray (SOG) digitized pixel data, is to sequentially compare two pixels spaced seven spaces apart. This comparison of two 7-bit samples is repeated each time the comparison selection increments one pixel in the direction of scan.