VPI

VIDEO PERCEPTION INCORPORATED

IPP3000R

CMOS RealTime Image Pre-Processor

25MHz

The IPP3000R is a uniquely programmed device which, when coupled with a Altera 10K10 PLD, (user supplied identified as IPP3000) provides extensive processing capabilites for use as a basic building block for new generation video based security systems. It is a video motion detector operating in real time and capable of discriminating degrees of motion as a basis for providing enhanced image motion detection. The IPP3000 uses a patented principle of locating edges in both the horizontal and vertical directions. The edges are uniquely processed to provide substantially improved results which minimizes false alarm conditions, while maximizing system sensitivity insuring positive detection. The image viewing area is subdivided into very small units (cells). The horizontal and vertical edge processed results are encoded into a single bit representing the boundary status of each cell. This approach provides a greatly reduced volume of data (128 times reduction) which represents the status of many pieces of the image. This condensed data format provides faster processing speed, as well as a significant reduction of support electronics.

A typical application requires digitized video data, one IPP3000R (up to eight multiplexed camera inputs), one PLD and two external RAM ICs, (MASK RAM optional). The IPP3000 stores a status representation of the reference image in external RAM. It then compares the real time representation of the image with the stored reference image and determines the degree of change. If the change exceeds a user selected tolerance for motion, an alarm output flag is set. This flag sets/resets each field of the image. An update of the reference image can be directed by an external timer or manual/computer-controlled directive. There are two user determined modes of external timer motion detection available. One selects change of the real time image from the reference image. The other detects only the new edge conditions (intruder boundary). The masking option allows the user to ignore specific areas of view. The IPP3000 supports up to eight multiplexed camera inputs, using RS170 cameras and a video digitizer, with a 7.5 image sample/second rate for each.

FEATURES

- Operates at 25 MHz Clock Rate
- Provides Real Time Image Processing
- Provides Discriminatin Motion Detection
- Filters Image Noise
- Provides up to 1024 x 1024 Processing Resolution
- Supports Camera-Based or External-Computer Usage
- Supports Dynamic DifferentiaThreshold Adjustment
- Supports Dynamic Motion Adjustment
- Supports Masking for Motion Data
- Supports Multiplexing of up to eight Cameras
- Provides Digital Motion Data for Image ID/Tracking
- Supports Multiplexing of Digital data on Video Signal

APPLICATIONS

- Intrusion Detection/Object Recognition
- Airport Flight Safety
- Military Perimeter Security
- Auto Speed Monitor
- Computer Based Object Tracking

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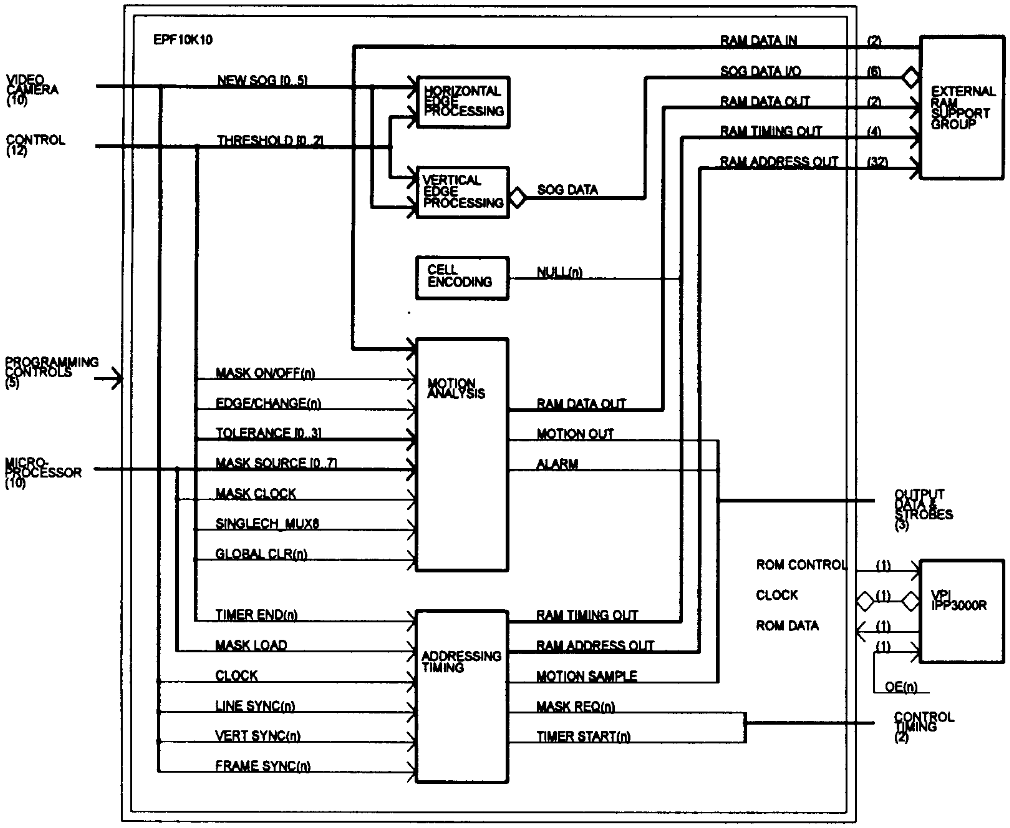
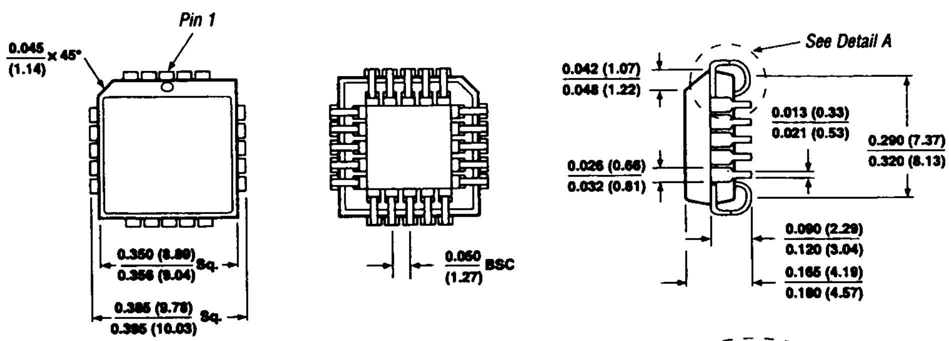
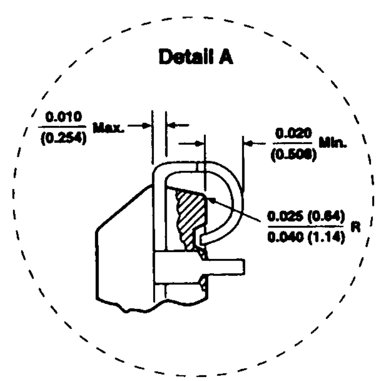
Simplified Block Diagram



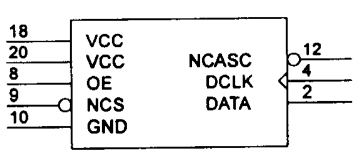
20-Pin Plastic J-Lead Chip Carrier (PLCC) PACKAGE CONFIGURATION

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only.





PIN-OUTS **FOR** THE **IPP3000R**



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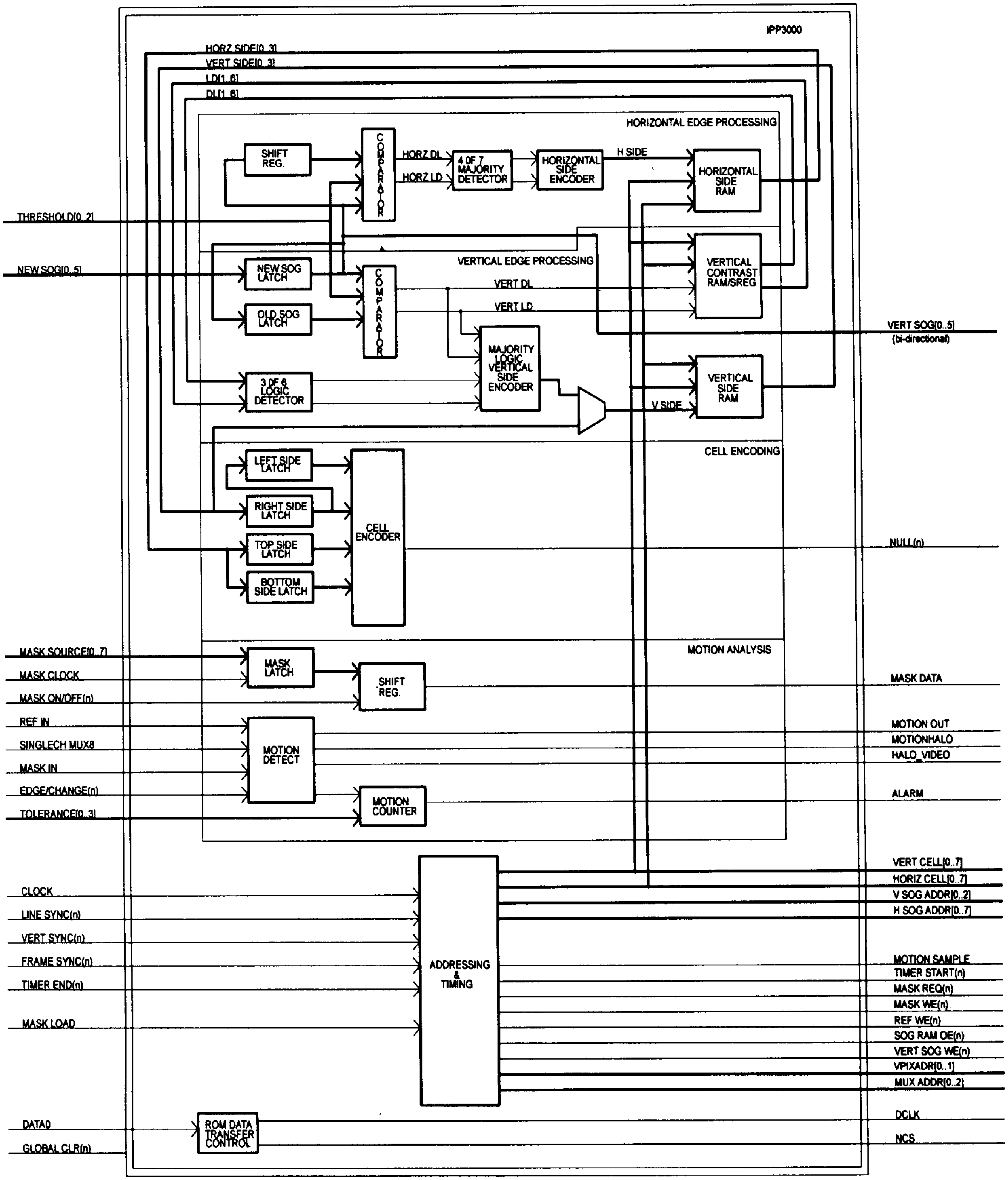
Functional Block Diagram



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Pin Assignment

(of Altera EPF10K10QC208 when configured as an IPP3000)

PIN	SIGNAL NAME	TYPE	PIN	SIGNAL NAME	TYPE
128	TIMER END(n)	Input	67	TIMER START(n)	Output
79	CLOCK	Input	115	MOTION OUT	Output
18	NEW SOG 0	Input	205	MOTION SAMPLE	Output
12	NEW SOG 1	Input	116	MASK REQ(n)	Output
13	NEW SOG 2	Input	169	ALARM	Output
147	NEW SOG 3	Input	45	VPIXADR 0	Output
16	NEW SOG 4	Input	134	VPIXADR 1	Output
17	NEW SOG 5	Input	162	H SOG ADDR 0	Output
27	THRESHOLD 0	Input	163	H SOG ADDR 1	Output
29	THRESHOLD 1	Input	164	H SOG ADDR 2	Output
31	THRESHOLD 2	Input	204	H SOG ADDR 3	Output
135	TOLERANCE 0	Input	99	H SOG ADDR 4	Output
30	TOLERANCE 1	Input	120	H SOG ADDR 5	Output
157	TOLERANCE 2	Input	101	H SOG ADDR 6	Output
136	TOLERANCE 3	Input	161	H SOG ADDR 7	Output
41	EDGE/CHANGE(n)	Input	69	V SOG ADDR 0	Output
24	SINGLECH/MUX8(n)	Input	70	V SOG ADDR 1	Output
148	MASK SOURCE 0	Input	131	V SOG ADDR 2	Output
142	MASK SOURCE 1	Input	149	VERT SOG 0	I/O
71	MASK SOURCE 2	Input	11	VERT SOG 1	I/O
75	MASK SOURCE 3	Input	19	VERT SOG 2	I/O
74	MASK SOURCE 4	Input	10	VERT SOG 3	I/O
141	MASK SOURCE 5	Input	144	VERT SOG 4	I/O
143	MASK SOURCE 6	Input	150	VERT SOG 5	I/O
187	MASK SOURCE 7	Input	208	SOG RAM OE(n)	Output
184	MASK CLOCK	Input	192	VERT SOG WE(n)	Output
186	MASK LOAD	Input	60	HORIZ CELL 0	Output
73	MASK ON/OFF(n)	Input	133	HORIZ CELL 1	Output
40	MASK IN	Input	132	HORIZ CELL 2	Output
119	REF IN	Input	121	HORIZ CELL 3	Output
80	GLOBAL CLR(n)	Input	172	HORIZ CELL 4	Output
183	LINE SYNC(n)	Input	111	HORIZ CELL 5	Output
78	VERT SYNC(n)	Input	112	HORIZ CELL 6	Output
127	FRAME SYNC(n)	Input	158	HORIZ CELL 7	Output
154	nCE	Input	47	VERT CELL 0	Output
155	DCLK	Input	189	VERT CELL 1	Output
156	DATA0	Input	198	VERT CELL 2	Output
105	nCONFIG	Input	63	VERT CELL 3	Output
108	MSEL0	Input	61	VERT CELL 4	Output
107	MSEL1	Input	200	VERT CELL 5	Output
2	CONF_DONE	I/O	207	VERT CELL 6	Output
52	nSTATUS	I/O	55	VERT CELL 7	Output
50	TMS	Input	62	MUX ADDR 0	Output
1	TCK	Input	199	MUX ADDR 1	Output
153	TDI	Input	46	MUX ADDR 2	Output
4	TDO	Output	68	MASK DATA	Output
51	nTRST	Input	196	NULL(n)	Output
			197	MASK WE(n)	Output
			104	REF WE(n)	Output
			175	MOTIONHALO	Output
			122	HALO VIDEO	Output

NOTE: Refer to the Altera EPF10K10QC208 data sheets for power and ground connections.

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SIGNAL DEFINITIONS

POWER&PROGRAMMING PINS *(see appropriate Altera data sheets)*

The following power pins must be connected to VCC

VCCINT

6, 23, 35, 43, 76, 77 106, 109, 117, 137, 145, 181

VCCIO

5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194

The following power return pins must be connected to ground.

GNDINT

21, 33, 49, 81, 82, 123, 129, 151,185

GNDIO

20, 32, 48, 59, 72, 91,124, 130, 152, 171,188, 201

nCE, MSELO, MSEL1, nTRST

These pins must be connected to ground.

nCONFIG, TMS, TCK, TDI

These pins must be connected to VCC.

DCLK

This pin must be connected to the DCLK pin of the IPP3000R. It provides the clock for data transfer from the IPP3000R to the PLD.

DATA0

This pin must be connected to the DATA pin of the IPP3000R. It provides data from the IPP3000R to the PLD.

nSTATUS

This pin must be connected to the OE (n) pin of the IPP3000R. It also must be connected to VCC through a 1K ohm resistor.

CONF DONE

This pin must be connected to the nCS pin of the IPP3000R. It also must be connected to VCC through a 1K resistor.

CLOCK & TIMING INPUTS

CLOCK

The pixel clock from the video camera supplies the clocking to the IPP. All input signals from the video camera transition on the positive going edge of CLOCK. The maximum clock rate is 25 MHz.

LINE SYNC (n)

This signal is supplied from the video camera. It controls the incrementing of the line counter within the IPP to control memory access addresses. It also terminates the pixel counter (for position within a horizontal line) of the IPP to permit adjustment to any line length within the IPP addressing limitations of 1024 pixels. This can be extended with cascaded operation.

VERT SYNC (n)

This input is supplied from the video camera. It controls the reset of address counters within the IPP to the start of a new image trace. This is the vertical retrace signal for interlaced camera mode and is the frame sync for non-interlaced mode. This must be connected to VCC for linear array camera operation.

FRAME SYNC (n)

Only interlaced mode camera operation utilizes this input; it must be connected to VCC for non-interlaced or linear array camera operation. This signal synchronizes the internal IPP counters to the video camera when employed.

MASK CLOCK

An external microprocessor supplies this clock during read operations from an external RAM (see Figure 1) to strobe the data being read from the RAM. These data are also latched by the IPP.

TIMER END (n)

When the timing of reference field storage update is controlled by an external timer, the negative going edge of the timer output initiates the synchronous loading of the IPP support Reference RAM at the start of a vertical retrace. This initiation signal may be asychronous. This loads the current image null status data (1 bit per cell) into the Reference RAM. The loading can be initiated by any other external control operation causing a negative going transition of this signal.

DATA INPUTS

NEW SOG [0..51

These input data are the pixel shades-of-gray (SOG) light intensity data from a digital video camera. Bit 0 is the least significant bit (lsb). This input range should be over the dynamic range of the image for best results. Video cameras having resolution greater than six bits can utilize the greater resolution to translate the IPP input to the dynamic six bit range.

REF IN

This input signal provides the null status of the current cell being internally addressed by the IPP from the data stored in the Reference RAM. A low state define a null status; a high state identifies a boundary condition. If a Reference RAM is not used, this input must be connected to either VCC or GND.

MASK IN

This input provides the mask status, of the current cell being internally addressed by the IPP, from the data stored in the Mask RAM. A low state defines a non-masked condition; a high state causes any motion indication to be ignored for that cell. If a Mask RAM is not used, this input must be connected to GND to enable motion detection.

MASK SOURCE [0..71

Mask data is supplied to the IPP by these inputs and is strobed by signal MASK CLOCK. Bit 0 is the lsb.

CONTROL INPUTS

THRESHOLD [0..2]

These inputs provide control to the comparators oftbe horizontal and vertical edge processing to provide a differential threshold. This must be cxceeded by the absolute difference of the two sample inputs of the comparator before contrast (DL or LD) is indicated. Bit 0 is the lsb. (See Table II and note 1).

TOLERANCE [0..3]

These inputs provide proload control to counters oftbe motion detector oftbe IPP. This provides a required count of the cells containing motion indications before an alarm status is indicated. Bit 0 is the lsb. (See Table I and note 1).

EDGE/CHANGE (n)

This input selects one of two modes of motion detection when the cell being monitored is not masked. In the CHANGE (low) mode, a motion cell count is detected if the current NULL (n) output indication does not match that provided by the REF IN input. In the EDGE (high) mode, a motion cell count is detected if the REF IN input is low and the NULL (n) output indication is high.

MASK ON/OFF (n)

In the OFF (low) mode of this input, there is no masking of data to the motion detector. In the ON (high) mode, the motion counter input is disabled from detecting additional counts where masked.

MASK LOAD

This signal initiates the conversion and loading of a field of MASK SOURCE [0..7] data (in eight bit format) to MASK DATA at the IPP output to the Mask RAM in single bit format. The loading process is synchronous with the image field address timing; the MASK LOAD input may be applied asychronously. Mask RAM loading is initiated as a result of a high input.

SINGLECH/MUX8 (n)

The user can select from multiplexed or non-multi-plexed motion detection operation. Single channel operation is selected with the signal in the high level. Comparisons of image boundary conditions are made on every other field. Multiplexed operation of eight channels is selected with the signal low. Comparisons of image boundary conditions are made on every field.

GLOBAL CLR (n)

The signal clears most of the internal latched elements when in the active low level. These internal latched elements will self initialize after a single field of operation.

DATA & FLAG OUTPUTS AND I/O

VERT SOG [0..5]

These I/O are the SOG data from the video camera latched and routed by the IPP to RAM. The latched samples written to the RAM are every fourth pixel corresponding to the left most pixel position within the cell for the horizontal scan line. Bit 0 is the lsb. Signal VERT SOG WE (n) causes the loading of these data.

NULL (n)

This output signal indicates the boundary. status of the currently accessed cell. It is a flag which is also used as data to the Reference RAM during a single field update; the frequency of this update is controlled by the TIMER END (n) input. Signal REF WE (n) causes the loading of this signal. A low level output defines a null status; a high level defines a boundary detection status of the cell. The data are valid at the negative going edge of DATA STROBE (n).

MASK DATA

This output signal is valid only during the single field of Mask RAM update initiated by the MASK LOAD input. Signal MASK WE (n) causes the loading of this signal. A high level indicates a masked condition for the accessed cell: a low level permits motion detection counting for the cell.

MOTION OUT

This output signal provides the motion status for the current accessed cell. A high level is a motion count; a low level is no indication of motion.

ALARM

This signal is a flag indicating the presence of motion in excess of that controlled by the TOLERANCE [0..3] inputs. The flag goes high if the motion count exceeds that defined by Table I; otherwise, it remains low. The flag indication remains active from the time of first detection of motion until the time that motion ceases.

MOTIONHALO

This output signal provides motion data representative of cell status. It also provides a halo around objects in motion when multiplexed with the analog video under control of signal HALO VIDEO (n). The video coax cable can be used to transmit motion data to a central location. The data can easily be removed from the multiplexed signal for further computer motion analysis.

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TIMING & CONTROL OUTPUTS

SOG RAM OE (n)

This timing signal enables the external Shades-Of-Gray RAM when in the active low level.

HALO VIDEO (n)

This signal controls the multiplexed selection of either digital motion data or analog video data through an external analog multiplexer. The digital data are output at MOTIONHALO.

TIMER START (n)

This signal is a negative going pulse (when active) to initiate an external timing device to begin a new timing interval. The external timer provides the TIMEREND (n) (low) input signal to the IPP at the completion of the timing interval. This low TIMER END (n) input causes the TIMER START (n) output to go low; consequently, this is a continuous process causing update of the Reference RAM data with a field of the current NULL (n) data on each occurrence.

MASK REQ (n)

This signal is a negative going pulse used to signal an external microprocessor (loading mask data) that the IPP is ready for another byte of mask data. It is used to synchronize the loading of mask data during a single image field.

MOTION SAMPLE

This positive going pulse provides timing for external processing of the IPP output MOTION OUT. This output may be latched on the positive going edge or during the high interval.

MASK WE (n)

IPP output MASK DATA are written to external RAM during the low interval of this signal.

REF WE (n)

IPP output NULL (n) data are written to external RAM during the low interval of this signal.

VERT SOG WE (n)

IPP output VERT SOG [0..5] data are written to external RAM during the low interval of this signal.

ADDRESS OUTPUTS

HORIZ CELL [0..7]

These data are the low order address inputs to the external RAM devices storing IPP output data NULL (n) and MASKDATA. Bit 0 is the lsb.

VERT CELL [0..7]

These data are the high order address inputs to the external RAM devices storing IPP outputs NULL (n) and MASK DATA. Bit 0 is the lsb.

H SOG ADDR [0..7]

These data are the low order address inputs to the external RAM device storing IPP output data VERT SOG [0..5]. Bit 0 is the lsb.

V SOG ADDR [0..2]

These data are the high order address inputs to the external RAM device storing IPP output data VERT SOG [0..5]. Bit 0 is the lsb.

VPIXADR [0.. II

These address outputs define the current vertical line address within a cell. Bit 0 is the lsb.

MUX ADDR [0..2]

These address outputs are field count. They determine the high order address applied to the external Reference RAM and Mask RAM. They can also be used to control the selection of an external video multiplexer.

Note 1.

The input can be dynamically changed asychronously; the resultant change will be initiated synchronously with the start of an image field.

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DESIGN IMPLEMENTATION

The IPP3000 function is implemented in an Altera EPF10K10QC208 Programmable Logic Device (PLD). IPP3000R is the designation for the Video Perception, Inc. Read-Only-Memory (ROM) device used to load the Altera PLD each time power is applied to the circuit. The operating PLD-ROM pair is hereafter designated an IPP3000.

GENERAL INFORMATION

The IPP3000, hereafter referred to as Image Pre-Processor (IPP), is a real time image processor which translates digital pixel data, received in the horizontal scanning pattern as transmitted by a video camera, into motion data useful for intrusion detection. It processes the horizontal scanned data to determine horizontal edge conditions. It controls the storing of vertical columns of pixel data to perform a pseudo scan in the vertical direction. It then determines vertical edge conditions. The edge data derived by horizontal and vertical edge processing are stored in RAM until all needed components of these data are available for encoding. It then retrieves these components to generate motion data. Mask data can be loaded into the support group RAM under control of the IPP and an external microprocessor (see Figure 1). Reference data can be loaded into the support group RAM through timer initiation of the IPP control. The mask data disables motion detection over a selection of the many regions of the image called cells. A motion counter detects motion indications of comparisons of stored and real time image data representations of these cells of the image (when not masked). This provides a count of the difference indications. A motion tolerance can be input to the IPP to establish a motion count level that will cause an alarm. When that count per field is exceeded, the alarm flag will be set. Address and timing is developed internally to control the external support group RAM. Figure 2 is a block diagram of the IPP connected to the external support group RAM. It illustrates the interface to the three basic RAM sections.

CELL STRUCTURE AND PROCESSING OVERVIEW

The IPP sub-divides the image viewing area into 4x4 pixel space regions called cells (see Figure 3). These cells are bounded by lines which sub-divide the image viewing area every four pixel spaces in both the horizontal and the vertical directions. The lines are along perimeter sides of these cells establishing 64K cells. The image is scanned in the horizontal direction by the natural scanning of the video camera along the perimeter sides of cells to detect edges in accordance with an algorithm to be defined later. Digitized pixel data occurring along the vertical perimeter sides of cells are accumulated in external RAM storage and pseudo scanned in the vertical direction in accordance with the same algorithm used in the horizontal direction. Each cell shares sides with the adjacent cells creating 5x5 pixel cell mattics (at 4x4 pixel spaces). Figure 4 illustrates this structure.

The horizontally detected edge status and the pseudo scanned vertically detected edge status, for each of the four sides, are evaluated. The four encoded sides are then applied to a cell boundary encoder which encodes the cell edge status (see Figure 5). If none of the sides has an edge indication, a null status output is provided. Otherwise, the output is a boundary indication within the cell. The IPP controls the RAM storage of in-process data developed to be used at a later interval; it retrieves these data at the proper timing as needed. The internal RAM used for development of vertical data requires eight horizontal scan lines of storage. The internal RAM used for development of horizontal data requires only four horizontal scan lines storage. This RAM is reused for follow-on scan lines; this technique requires relatively small memory storage space. The IPP responses to input controls TOLERANCE and THRESHOLD are defined in Table I and Table II.

EDGE DETECTION

Edge detection is a multi-step process. The first step, in both the horizontal and vertical edge processing of Shades-Of-Gray (SOG) digitized pixel data, is to sequentially compare two pixels spaced seven spaces apart. This comparison of two 7-bit samples is repeated each time the comparison selection increments one pixel in the direction of scan. A contrast indication, either DL or LD, is registered when the difference value of the two pixels of the sample exceed the absolute value of a differential threshold resulting from external control. The second step is to evaluate both the DL and the LD contrast indications with a four of seven majority logic circuit to determine edge locations. At the first occurrence of this majority, a location of the edge and the contrast type are registered. At the same time, the history of contrast indications is reset to assure that the frequency. of edge indications will only be once per cell. The majority logic circuit filters image noise input; it also enhances edge detection. The third step is to encode the cell side data. The fourth step is to store the side data into internal RAM until data from other sides of the cell are available.

DATA TRANSFER TIMING

Data are placed in internal storage until the proper timing to retrieve them for use in the processing. Figures 6 and 7 are tinning diagrams of the NULL(n) data development occurring only on cell line number 3.

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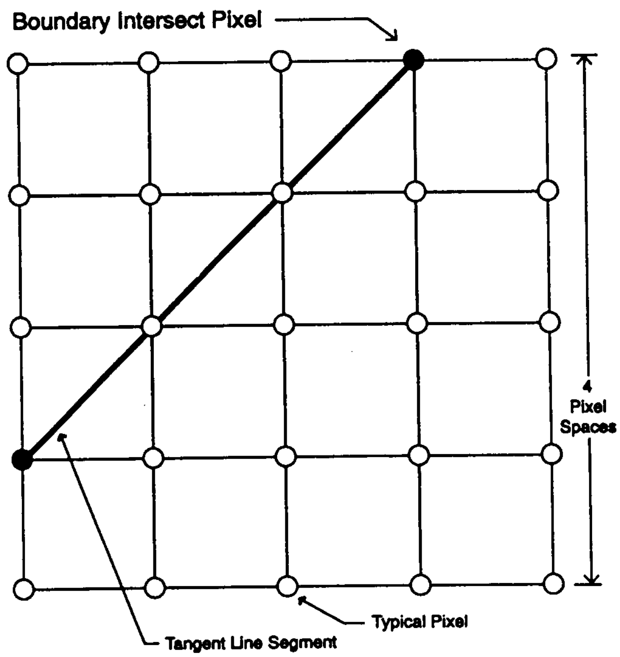
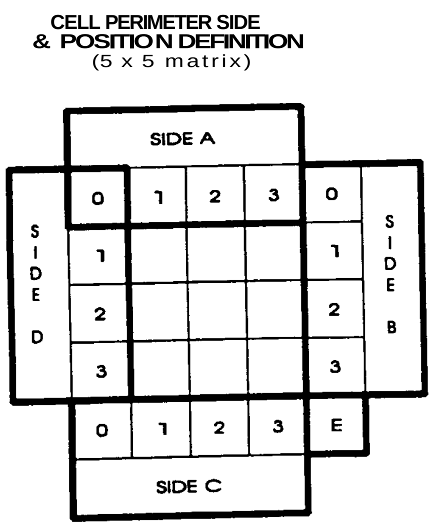


Figure 6
Pixel Matrix of a Cell



Note the overlap of perimeter position AO and DO. This leaves position E un-attached to a side. Therefore, sides A, B, C, and D plus position E define the cell perimeter Intersection points.

Figure 7

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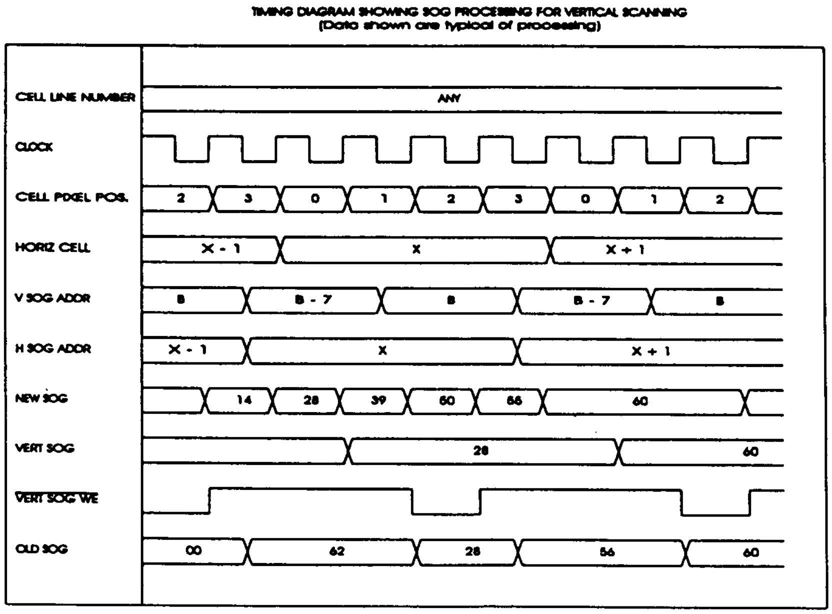
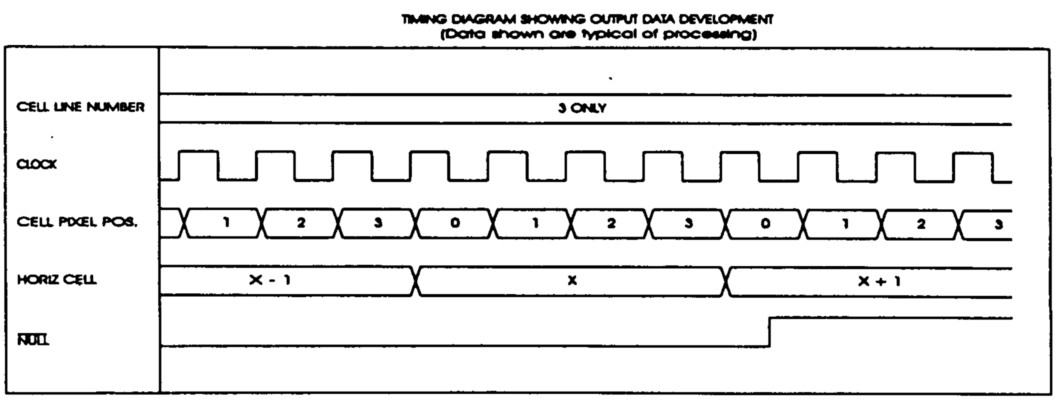


X = HORIZ CELL ADDRESS B = VERTICAL LINE ADDRESS Figure 8



X = HORIZ CELL ADDRESS Figure 9

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Table I

TOLERANCE CONTROL
COUNTS REQUIRED
TO SET ALARM

BINARY TOLERANCE NUMBER	DECIMAL COUNTS TO ALARM
0000	5
0001	7
0010	9
0011	13
0100	21
0101	33
0110	49
0111	73
1000	113
1001	161
1010	257
1011	385
1100	577
1101	897
1110	1281
1111	1921

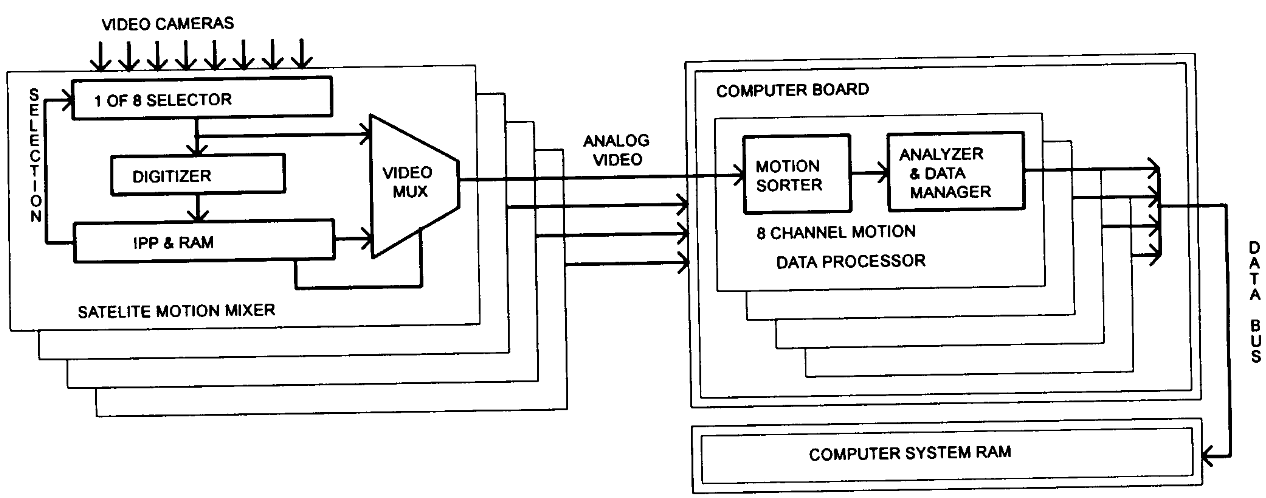
Table II

THRESHOLD CONTROL
COMPARATOR DIFFERENCE
BEFORE CONTRAST DETECTION

BINARY THRESHOLD NUMBER	BINARY DIFFERENCE REQUIRED
000	000010
001	000100
010	000110
011	001000
100	001100
101	010000
110	011000
111	100000

APPLICATION:

MOTION ANALYZING SYSTEM



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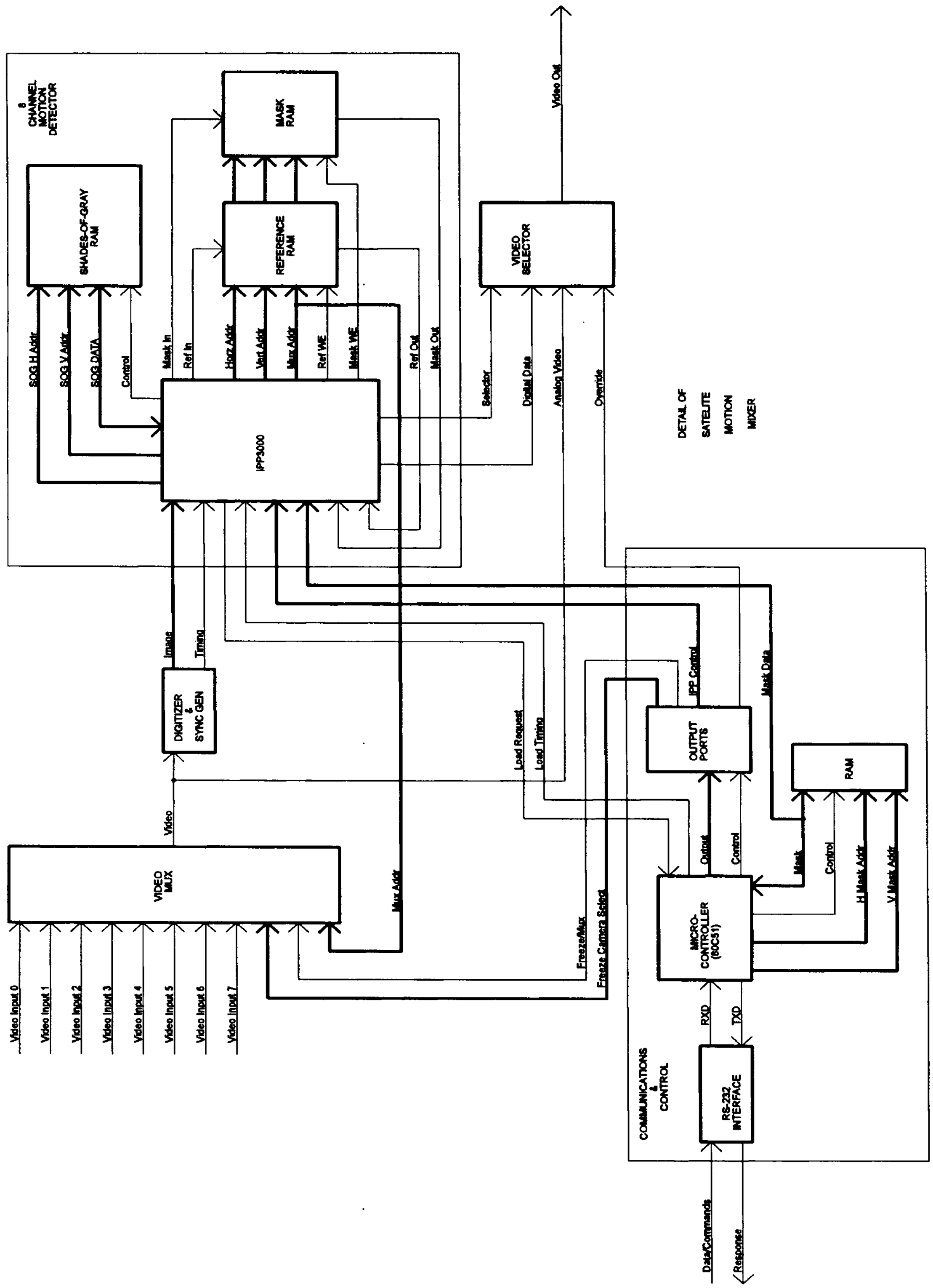

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OPERATING PLATFORMS

2 - Dimension Video Camera
Liner Array Video Camera
Computer
Bank Equipment
Other Specialized Equipment

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